## AMENDMENTS TO THE CLAIMS

Claims 1-83. (Cancelled)

84. (New) An inductive element comprising:

a semiconductor substrate including a cavity and having at least one semiconductor wall formed within said cavity, said semiconductor wall including a top surface;

an oxide insulating layer provided on said top surface; and

a conductive element located over said oxide insulating layer, said conductive element being supported by said semiconductor wall and including at least one loop.

85. (New) The inductive element of claim 84, wherein said semiconductor substrate has a plurality of semiconductor walls.

86. (New) The inductive element of claim 85, wherein said substrate has a center portion, and said semiconductor walls extend radially from said center portion.

87. (New) The inductive element of claim 84, wherein said semiconductor wall includes silicon.

88. (New) The inductive element of claim 84, wherein said semiconductor wall has a height of about 200 microns.

89. (New) The inductive element of claim 84, wherein said oxide insulating layer has a thickness of about 100 Angstroms to about 500 Angstroms.

90. (New) The inductive element of claim 84, further comprising a resist material formed between said at least one semiconductor wall and said semiconductor substrate.

91. (New) The inductive element of claim 84, wherein said loop has a thickness of about 0.3 microns to about 0.5 microns.

92. (New) The inductive element of claim 84, wherein said loop includes copper.

93. (New) The inductive element of claim 84, wherein said loop has a spiral configuration.

94. (New) The inductive element of claim 84 further comprising a barrier layer over said oxide insulating layer, said barrier layer is formed of a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

95. (New) The inductive element of claim 84, wherein said semiconductor substrate is one of a silicon substrate, a germanium substrate and a gallium arsenide substrate.

96. (New) A semiconductor device having a substrate and a cavity structure, a portion of said substrate being in contact with said cavity, said device comprising:

a plurality of semiconductor support elements provided in said cavity, said plurality semiconductor support elements extending radially from a center portion of said cavity structure and having a height of about 200 microns, said plurality of semiconductor support elements including a top surface;

an insulating layer provided on said top surface;

a barrier layer provided over said insulating layer; and

at least one electrically conductive loop formed over said barrier layer, said electrically conductive loop being supported by said semiconductor support elements.

97. (New) The device of claim 96, wherein said semiconductor support elements form an angle with said electrically conductive loop.

98. (New) The device of claim 97, wherein said angle is a 90° angle.

99. (New) The device of claim 96, further comprising a resist material formed in said cavity structure, between said semiconductor support element and said substrate.

100. (New) The device of claim 96, wherein said electrically conductive loop has a thickness of about 0.3 microns to about 0.5 microns.

101. (New) The device of claim 96, wherein said electrically conductive loop has a spiral configuration.

102. (New) The device of claim 96 further comprising a top insulating layer over said electrically conductive loop.

103. (New) The device of claim 96, wherein said semiconductor support elements have a wall configuration.

104. (New) The device of claim 96, wherein said semiconductor support elements have a column configuration.

105. (New) An inductive element comprising:

a semiconductor substrate including a cavity and having a plurality of semiconductor walls formed in said cavity, said semiconductor walls including silicon and extending radially from a center portion of said semiconductor substrate;

a silicon oxide layer provided on top surfaces of said semiconductor walls; and

at least one spiral loop located over said silicon oxide layer, said at least one spiral loop being supported by said semiconductor walls and having a thickness of about 0.3 microns to about 0.5 microns.

106. (New) The inductive element of claim 105, wherein said semiconductor walls have a height of about 200 microns.

107. (New) The inductive element of claim 105 further comprising a barrier layer over said silicon oxide layer, said barrier layer being formed of a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

108. (New) The inductive element of claim 105, wherein said semiconductor substrate is one of a silicon substrate, a germanium substrate and a gallium arsenide substrate.

109. (New) An inductive element comprising:

a semiconductor substrate including a cavity and having a plurality of semiconductor columns formed in said cavity, said semiconductor columns including silicon and extending radially from a center portion of said semiconductor substrate;

a silicon oxide layer provided on top surfaces of said semiconductor columns; and

at least one spiral loop located over said silicon oxide layer, said at least one spiral loop being supported by said semiconductor walls and having a thickness of about 0.3 microns to about 0.5 microns.

110. (New) The inductive element of claim 109, wherein said semiconductor columns have a height of about 200 microns.

111. (New) The inductive element of claim 109 further comprising a barrier layer over said silicon oxide layer, said barrier layer being formed of a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

112. (New) The inductive element of claim 109, wherein said semiconductor substrate is one of a silicon substrate, a germanium substrate and a gallium arsenide substrate.